

### Features

- First differential Spread Spectrum for PCI-Express and Fully Buffered -DIMM applications
- Low cycle-cycle jitter of 15 ps, lowest in industry
- -0.5% down spread option
- Reduces EMI up to -16 dB
- 100 MHz and 200 MHz output frequencies
- Industrial temperature range, -40 to 85 °C
- High frequency stability of  $\pm 50$  PPM (Spread = Off)
- Available in two industry standard packages: 5.0 x 3.2 x 0.75 mm and 7.0 x 5.0 x 0.90 mm
- All-silicon device with outstanding reliability of 2 FIT, 10x improvement over quartz-based devices, enhancing system MTBF
- Ultra short lead time
- Please refer to SiT9002 datasheet for other frequencies (up to 800 MHz) and signaling levels (LVPECL, LVDS, CML)
- Please refer to SiT9102 datasheet for non-spread spectrum requirements

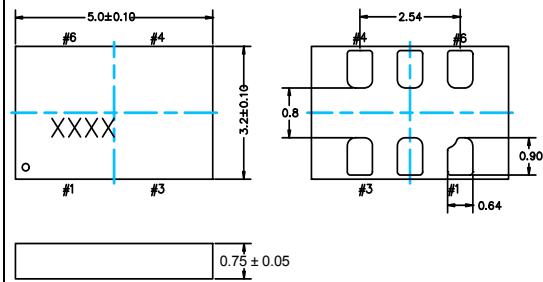


### Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	–	100	–	MHz	
		–	200	–	MHz	
Frequency Tolerance	F_tol	-50	–	+50	PPM	Spread Spectrum is off. Inclusive of: Initial tolerance, operating temperature, rated power, supply voltage change, load change, aging (1st yr @25°C), shock and vibration.
Aging	Ag	-1.0	–	1.0	PPM	1st year at 25°C
Storage Temperature Range		-55	–	+125	°C	
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage	Vdd	2.25	2.5	2.75	V	
		2.97	3.3	3.63	V	
Current Consumption	Idd		73	80	mA	Vcc = 3.3V or 2.5V. Excluding load termination current
Standby Current	I_std	–	–	10	μA	
Duty Cycle	DC	45	50	55	%	
Rise/Fall Time	Tr, Tf	200	280	375	ps	Vdd = 3.3V, 20% - 80% Vdd level
		200	300	400	ps	Vdd = 2.5 V, 20% - 80% Vdd level
Output High Voltage	VOH	0.6	0.75	0.95	V	50 Ohm termination to GND, see figure 1.
Output Low Voltage	VOL	0.0	–	0.5	V	
Pk-Pk Output Voltage Swing	Vsw	600	750	950	mV	
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE or Spread Disable
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE or Spread Disable
Startup Time	T_osc	–	–	10	ms	Measured from the time Vdd reaches its rated minimum value
Cycle-Cycle Jitter	T_jitt	–	10	16	ps	f = 100 MHz, Spread = -0.5%, Vdd = 3.3V
		–	10	15	ps	f = 200 MHz, Spread = -0.5%, Vdd = 3.3V
		–	9	19	ps	f = 100 MHz, Spread = -0.5%, Vdd = 2.5V
		–	9	15	ps	f = 200 MHz, Spread = -0.5%, Vdd = 2.5V

■ Dimensions, Pin Description and Land Pattern

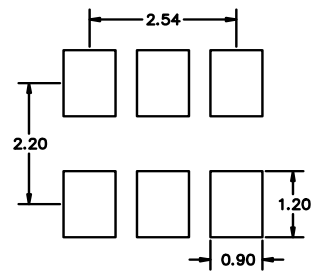
Dimensions (Unit: mm)<sup>[1]</sup>  
**5.0 x 3.2 x 0.75 mm**



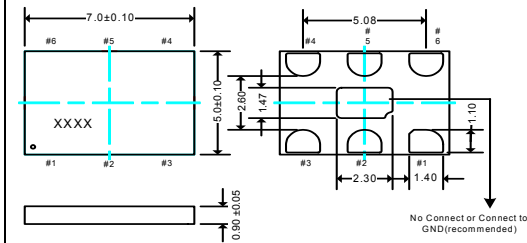
Pin Map	
Pin	Connection
1	OE / Spread Disable
2	No Connect
3	GND
4	OUT+
5	OUT-
6	Vdd

Pin #1 Functionality	
OE	
H or Open;	specified frequency output
L:	output is high impedance
SD	
H or Open;	Spread = ON
L:	Spread = Off (weak pull down)

Recommended Land Pattern (Unit: mm)<sup>[2]</sup>



Dimensions (Unit: mm)<sup>[1]</sup>  
**7.0 x 5.0 x 0.90 mm**



Recommended Land Pattern (Unit: mm)<sup>[2]</sup>

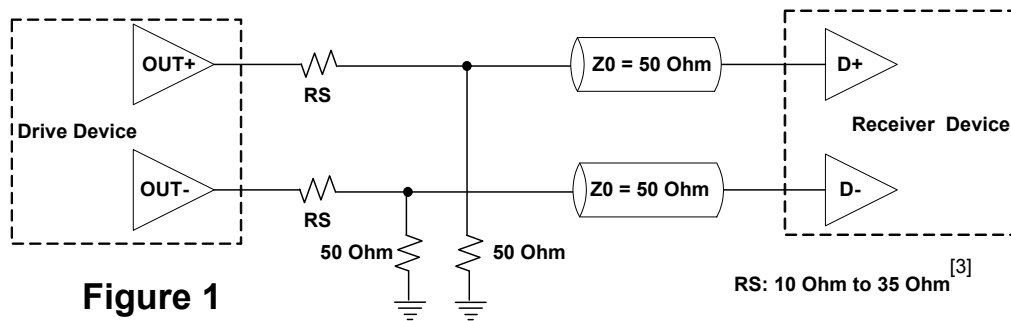
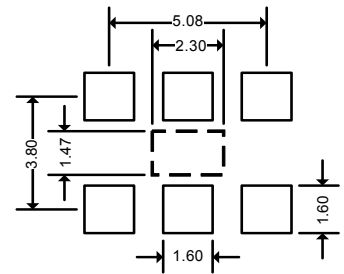


Figure 1

RS: 10 Ohm to 35 Ohm<sup>[3]</sup>

Notes:

- XXXX top marking denotes manufacturing lot number.
- A capacitor of value 0.1μF between Vdd and GND is recommended.
- All the tests are done with RS = 20 Ohm (recommended).

Ordering Part number	Frequency (MHz)	Package size (mm)	Vdd (V)	Feature Pin
SiT9002AI-433N33EO100.00000T	100	7.0 x 5.0 x 0.90	3.3	OE
SiT9002AI-433N33DO100.00000T	100	7.0 x 5.0 x 0.90	3.3	SD
SiT9002AI-433N25EO100.00000T	100	7.0 x 5.0 x 0.90	2.5	OE
SiT9002AI-433N25DO100.00000T	100	7.0 x 5.0 x 0.90	2.5	SD
SiT9002AI-423N33EO100.00000T	100	5.0 x 3.2 x 0.75	3.3	OE
SiT9002AI-423N33DO100.00000T	100	5.0 x 3.2 x 0.75	3.3	SD
SiT9002AI-423N25EO100.00000T	100	5.0 x 3.2 x 0.75	2.5	OE
SiT9002AI-423N25DO100.00000T	100	5.0 x 3.2 x 0.75	2.5	SD
SiT9002AI-433N33EO200.00000T	200	7.0 x 5.0 x 0.90	3.3	OE
SiT9002AI-433N33DO200.00000T	200	7.0 x 5.0 x 0.90	3.3	SD
SiT9002AI-433N25EO200.00000T	200	7.0 x 5.0 x 0.90	2.5	OE
SiT9002AI-433N25DO200.00000T	200	7.0 x 5.0 x 0.90	2.5	SD
SiT9002AI-423N33EO200.00000T	200	5.0 x 3.2 x 0.75	3.3	OE
SiT9002AI-423N33DO200.00000T	200	5.0 x 3.2 x 0.75	3.3	SD
SiT9002AI-423N25EO200.00000T	200	5.0 x 3.2 x 0.75	2.5	OE
SiT9002AI-423N25DO200.00000T	200	5.0 x 3.2 x 0.75	2.5	SD

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