Termination Recommendations for SiTime Single-Ended Oscillators

1 Introduction

Printed Circuit Boards (PCB) are the most common media used for mounting oscillators and routing clock signals in a system level board design. At higher frequencies, the PCB traces should be considered as transmission lines rather than simple wire connections.

SiTime oscillators have low output impedances. An impedance mismatch will occur when they are connected to devices with high input impedances. If the signal trace is not properly terminated, clock signals will be reflected from the load towards the source and cause distortions such as ringing, overshooting, and undershooting.

Equation 1 describes the condition at which trace termination is required.

$$L \geq \left(\frac{T_R}{N \times t_{pd}} \right)$$

Equation 1. Maximum trace length before termination is required

L = Trace Length
T_R = Rise Time (10% to 90% of the signal)
T_{pd} = Propagation Delay per unit length of trace
N = 2

From equation 1, we can observe that if the trace length is greater than or equal to the Rise Time (T_R) of the clock signal divided by two times the Propagation Delay (T_{PD}), then signal reflections will occur if the trace is not terminated properly. For example, assuming that the propagation delay of the signal is 150ps/inch and the rise time of the clock is 1 ns, then termination is required if the trace is longer than 3.3 inches.

In conservative designs, the user may increase the value of N (e.g. N=3) in the equation, further reducing the maximum trace length before termination is needed.

2 Clock Termination Recommendation

Output trace length should be kept as short as possible to avoid signal distortion caused by transmission line effects. If longer traces are unavoidable, the user should terminate the clock traces. SiTime recommends series termination for single-ended clocks.

Series termination is constructed by inserting a small resistor in series with the trace as close to the source as possible (see Figure 1).

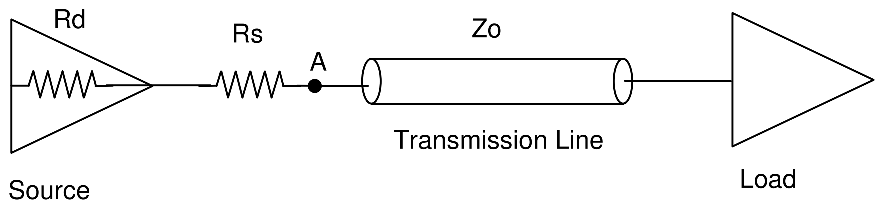

Figure 1. Series Termination

The value of the series termination resistor (Rs) plus the output impedance of the clocking device (Rd) should be equal to impedance of the transmission line (Zo). The typical output impedance for the SiT8002, SiT8102, and SiT9001 clock generators is 25 Ω. Therefore, a 25 Ω series termination resistor would be appropriate if the characteristic impedance of the transmission line is 50 Ω.

With such a configuration, the signal from the source will travel along the trace until it reaches the load. Typical loads have very high input impedances (in the range of mega-ohms), so no energy will be absorbed and the entire signal is reflected back to the source. Because the impedance at the source is now matched to that of the transmission line, no further reflections will occur.

Series termination is an economical way to terminate clock signals. It is simple, inexpensive, consumes very little power, and requires little board space. Series termination is suitable for driving a lumped load at the end of the trace. However, it is not recommended for driving distributed loads along the trace.

Consider the signal at point A in Figure 1. Since Rs + Rd = Zo, the voltage level at point A is exactly one-half (50%) of the voltage at the source when the signal is travelling outwards towards the load. Full voltage at point A is reached only then the signal is reflected back from the load (i.e., twice the propagation delay time from source to load). Such signal integrity issues exist for all positions along the trace except at the load end.

2.1 Series Termination for Multiple Loads

If the clock has to drive multiple loads, series termination can be implemented in two different ways, as shown in Figures 2 and 3.

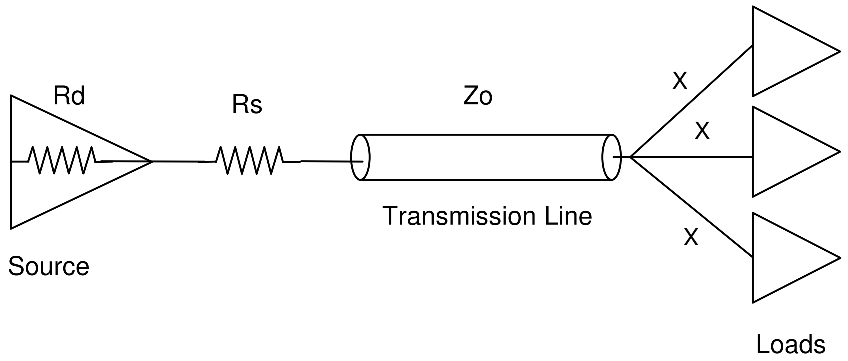

Figure 2. Series Termination with Multiple Loads Lumped at End of Trace

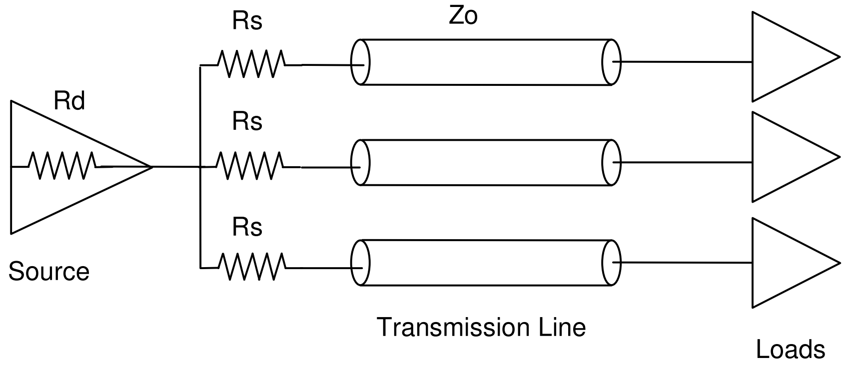

Figure 3. Series Termination from Single Source to Separate Loads

The loads in Figure 2 are located closely together at the end of the trace; therefore they can be treated as a single lumped load. The three loads in the figure are connected in a "star" formation and the "star" trace length X, must satisfy equation 1 with the value of N set to 5 or higher. Using the same assumptions in section 1 (propagation delay of the signal =150ps/inch, clock rise time = 1 ns, and N = 5), X can be calculated to be 1.3 inches or shorter.

If the "star' trace length is longer than X, then the loads cannot be considered as a lumped load. Each load must be driven via its own series termination resistor as shown in Figure 3. The value of Rs in Figure 3 is dependent on the number of parallel paths used in the system. For a system with 3 parallel paths, Rs is 38.4Ω if Rd = 25Ω and Zo = 50Ω. If there are only 2 parallel paths, Rs is 31Ω. For systems with different values of Rd or Zo, refer to the appendix for a discussion on how Rs can be calculated.

2.2 Low-Pass Filter Effect of the Series Termination

The Rd of the source, together with the series termination resistor Rs, and the input capacitance of the load, can be considered as a low-pass filter. Assuming that Rd and Rs are both 25 Ω, and the input of the load is 10 pF, a low-pass filter with a corner frequency of 318 MHz is formed.

For most applications, the corner frequency of this filter is high enough to cause no signal degradation. However, the user must monitor the load capacitance closely to ensure that the corner frequency stays comfortably above the operating range of the clock.

3 Conclusion

This application note contains signal termination recommendations for single-ended SiTime clock oscillators. Judicial usage of this information would allow users to achieve good clock signal integrity in their printed circuit boards.

Appendix

This appendix explains how the value of series termination resistor, Rs can be calculated in a system where a single clock output is used to drive multiple separate loads. Figure 4 is the AC equivalent schematic of Figure 3.

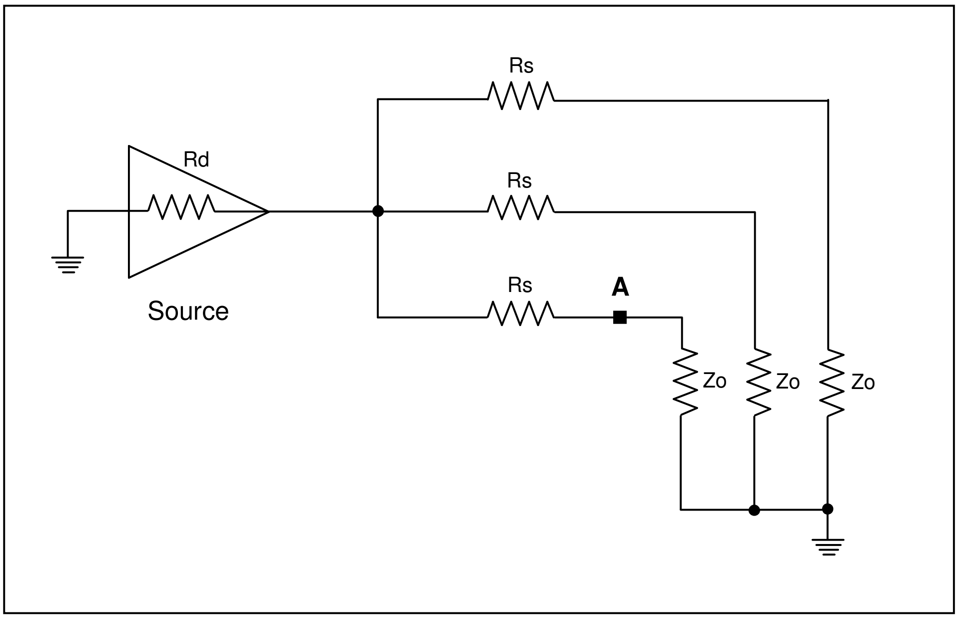

Figure 4. AC Equivalent schematic of Figure 3

Consider point A in the figure. To its right, point A sees a resistance of Zo. To its left, point A observes a resistance consisting of:

$$Rs + (Rd \,||\, (Rs + Zo) \,||\, (Rs + Zo))$$

Equating both sides of point A yields the following formula:

$$Zo = Rs + (Rd \,||\, (Rs + Zo) \,||\, (Rs + Zo)) \qquad \text{Equation 2}$$

If we substitute Zo = 50 and Rd =25 into Equation 2 and solve for Rs, we will find that Rs is equal to 38.4. Note that Equation 2 only covers a system with 3 separate loads. Use Equation 3 for a system with N parallel loads.

$$Zo = Rs + (Rd \,||\, Rx) \qquad \text{Equation 3}$$

where $Rx = (Rs + Zo) / (N-1)$

SiTime Corporation
990 Almanor Avenue
Sunnyvale, CA 94085
USA
Phone: 408-328-4400
http://www.sitime.com